**A NEW REDUCED SWITCH COUNT PULSE WIDTH MODULATED MULTILEVEL INVERTER**

**ABSTRACT**

The paper develops a new topology for a single phase cascaded H- Bridge multilevel inverter (CHB MLI) with a focus to reduce the number of power switching devices in the path for the flow of current. The philosophy combines an array of series connected voltage sources on either side of an H- bridge inverter to derive the new configuration for the MLI. It allows a Multicarrier Pulse Width Modulation (MCPWM) approach to the process of generating the pulses for synthesizing the PWM output voltage. The use of a smaller number of switches to reach the output voltage show cases the ability of the modular architecture to expand the scope of the CHBMLI. The architecture of a Field Programmable Gate Array (FPGA) fosters to realize its implementation and validate the simulated results over a range of modulation indices. The performance draws a new directive in the choice of a particular topology for the MLI to suit applications in the real world.

**BLOCK DIAGRAM FOR PROPOSED SYSTEM**



Fig. 1. Generalized topology .

**DESIGNG SOFTWARE AND TOOLS:**

MAT LAB /SIMULATION Software and simu power systems tools are used. Mainly control system tools, power electronics and electrical elements tools are used.